High Temperature Experiments Using Programmable Transistor Array

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Abstract—Temperature and radiation tolerant electronics, as well as long life survivability are key capabilities required for future NASA missions. Current approaches to electronics for extreme environments focus on component level robustness and hardening. Compensation techniques such as bias cancellation circuitry have also been employed. However, current technology can only ensure very limited lifetime in extreme environments. This paper presents a novel approach, based on evolvable hardware technology, which allows adaptive in-situ circuit redesign/reconfiguration during operation in extreme environments. This technology would complement material/device advancements and increase the mission capability to survive harsh environments. The approach is demonstrated on a mixed-signal programmable chip, which recovers functionality until 280°C. We show in this paper the functionality recovery at high temperatures for a variety of circuits, including rectifiers, amplifiers and filters.

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1. INTRODUCTION

In-situ planetary exploration requires extreme-temperature electronics able to operate in low temperatures, such as below –220°C on Neptune (-235°C for Triton and Pluto) or high temperatures, such as above 470°C as needed for operation on the surface of Venus. Extrapolations of current developments indicate that hot electronics technology for >400°C environments may not be ready in time for the 2006-2007 missions, except possibly for "grab-and-go" or "limited life" operations [1]. For extended missions, innovative approaches are needed. Terrestrial applications include combustion systems, well logging, nuclear reactors and dense electronic packages.

The maximum working temperature for semiconductors can be estimated from their intrinsic carrier density, which depends on the band-gap of the material. When the intrinsic density reaches the doping level of the devices, electrical parameters are expected to change drastically [2]. For the high-voltage regime (1000V), the theoretical limit for silicon is 150°C; for discrete devices below 100V, it is expected about 250°C [2]. Materials used up to 300°C include bulk silicon and silicon-on-insulator (SOI) technologies; for higher temperatures, gallium arsenide (GaAs), silicon carbide (SiC), and diamond show promise, and devices have been demonstrated at 500°C [3]. A survey of high-temperature effects and design considerations is found in [4]. A review of the physical limits and lifetime limitations of semiconductor devices at high-temperatures is found in [2].

In addition to material/device solutions, circuit solutions for the compensation of the effects of temperature have also been employed. Circuit solutions that compensate offset voltage and current leakage problems are described for example in [3], where several circuit topologies for high-

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temperature design, including a continuous-time auto-zeroed OpAmp and an A/D circuit that uses error suppression to overcome high-temperature leakages, are given. Another circuit for high-temperature operation with current leakage compensation is presented in [5]. Bias cancellation techniques for high-temperature analog application are presented in [6].

All the above solutions are fixed circuit design solutions, and satisfy the operational requirements only over a given temperature range. Once the limits of the range are exceeded, the performance deteriorates and cannot be recovered. In this paper, we propose the use of reconfigurable chips, which allow for a large number of topologies to be programmed, some more suitable for high-temperature. The interconnections between components can be changed, and new circuits can be configured, in an arrangement that uses the on-chip components/devices *at the new operational point on their characteristics*. In essence, a new design process takes place automatically, in-situ, under the control of a search algorithm. The configurations could be determined either before launch - part of the original design (which would identify good configurations and store them in a memory) - or in-situ. At the higher temperatures, once the performance of the current topology starts to deteriorate, the system would switch to a more suitable topology.

Reconfiguration can be controlled by evolutionary algorithms, a research area called Evolvable Hardware (EHW). Evolvable hardware technology is particularly significant to future NASA autonomous systems, providing on-board resources for reconfiguration to self-adapt to situations, environments and mission changes. It would enable future space missions using concepts of spacecraft surviving in excess of 100 years as well as electronics for temperatures over 460°C as encountered on the surface of Venus which pose challenges to current electronics. In addition, this technology can be used to reduce massive amounts of sensor data to lean data sent to centralized digital systems.

As part of an effort to develop evolution-oriented devices for Evolvable Hardware experiments, we designed and fabricated a series of Field Programmable Transistor Array (FPTA) chips in 0.5 micron and 0.18 micron bulk CMOS. These chips are reconfigurable at transistor level and were used to demonstrate on-chip evolution/synthesis of a variety of conventional building blocks for electronic circuits such as logical gates, transconductance amplifiers, filters, Gaussian neurons, data converters, etc [7], [8].

We present results on using evolution to recover the functionality of FPTA-mapped circuits affected by changes in temperature In this paper we present a more detailed account of the evolutionary recovery, and explain how temperature degradation can fundamentally impact the intended function of the IC. The examples chosen include analog circuits whose behavior deteriorates as the temperature increase, thus totally altering the intended analog function. Evolution is able to find alternate circuits that perform correctly at the higher temperature.

The paper is organized as follows: Section 2 reviews the concept of evolutionary circuit design; Section 3 presents the details on a FPTA-2 chip developed as an evolution-oriented architecture for reconfigurable hardware, and introduces the experimental high temperature testbed. Section 4 presents experiments that illustrate that evolution-guided reconfiguration can recover functionality deteriorated/altered by increased temperature. Section 5 presents a discussion on the behavior of the switches of the FPTA-2 chip at higher temperatures. Section 6 concludes the work.

2. EVOLUTIONARY CIRCUIT DESIGN

The idea behind evolutionary circuit synthesis/design and evolvable hardware is to employ a genetic search/optimization algorithm that operates in the space of all possible circuits and determines solution circuits with desired functional response (here the word synthesis is used in most general sense). The genetic search is tightly coupled with a coded representation of the candidate circuits. Each circuit gets associated a “genetic code” or chromosome; the simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. Synthesis is the search in the chromosome space for the solution corresponding to a circuit with a desired functional response. The genetic search follows a "generate and test" strategy: a population of candidate solutions is maintained each time; the corresponding circuits are then evaluated and the best candidates are selected and reproduced in a subsequent generation, until a performance goal is reached. In this project, since device models at extreme temperature are not available, circuit evaluation is done directly in reconfigurable hardware, called *intrinsic*. More details on Evolutionary Circuit Design can be found in [7-9].

3. STRUCTURE OF EVOLVABLE SYSTEMS

An evolvable hardware system is constituted of two main components: reconfigurable hardware (RH) and an evolutionary processor (EP) that acts as a reconfiguration mechanism. In the evolvable systems we built for this effort, the EP was implemented and ran on a stand-alone DSP board. The RH was embodied in the form of a Field Programmable Transistor Array (FPTA-2) architecture, a custom made chip fabricated in silicon. This section will refer to the general characteristics of the two components and will also describe the Evolvable System testbed for high temperature experiments.

3.1 The FPTA

The FPTA is an evolution-oriented reconfigurable architecture (EORA). Important characteristics needed by evolution-oriented devices are *total accessibility*, needed in order to provide evolutionary algorithms the flexibility of testing in hardware any chromosomal arrangements, some of which may be dangerous for existing commercial devices (may lead to internal bus allocation conflicts and burn the chip) and thus forbidden, *granularity at low level* (here transistor) allowing evolution to choose/construct the most suitable building block for certain system, and *transparency*, which enables users to have access to internal device information, etc.

The Field Programmable Transistor Array (FPTA) is such an EORA with configurable granularity at the transistor level. It can map analog, digital and mixed signal circuits. The architecture is cellular, with each cell having a set of transistors, which can be interconnected by other "configuration transistors". For brevity, the "configuration transistors" are called switches. However, unlike conventional switches, these can be controlled for partial opening, with appropriate voltage control on the gates, thus allowing for transistor-resistor type topologies.

Cells are interconnected to local neighbors with switches. A variety of simple circuits can be mapped onto this device or on multiple devices by cascading them. Its design was inspired by observing a variety of analog designs in which transistors often come in rows of pairs of transistors (for various current mirrors, differential pairs etc.), and have an average of four rows between VDD and ground. More rows can be ensured cascading cells, while fewer rows can be mapped by closing some switches to bypass rows.

The FPTA-2 is a third generation of reconfigurable chips designed at JPL, consisting of an 8x8 array of re-configurable cells. It was fabricated using TSMC 0.18u/1.8V technology. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 1 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The re-configurable circuitry consists of 14 transistors connected through 44 switches. The re-configurable circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its north, south, east and west neighbors. This is the first mixed-signal programmable array, FPMA, in the sense that its cells can be configured as both analog and digital circuitry; with its 64 cells it can configure more Operational Amplifiers (OpAmps) than the largest commercial Field Programmable Analog Array (FPAA) chip (which contains only 20 OpAmps).

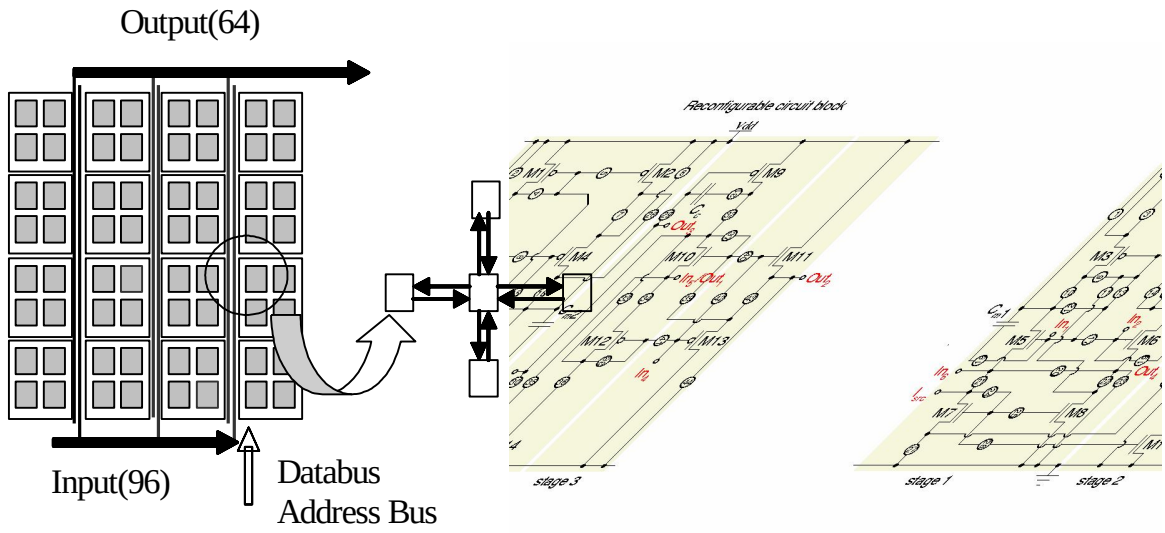


Figure 1: FPTA 2 architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

3.2 A stand-alone board-level evolvable system

A complete stand-alone board-level evolvable system (SABLES) was built by integrating the FPTA-2 and a DSP implementing the EP as shown in Figure 2. The system is connected to the PC only for the purpose of receiving specifications and communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is very fast with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zif socket attached to a metal electronics board to perform extreme temperature experiments. The evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 to 200 generations require only 20 seconds.

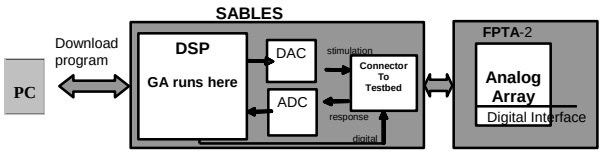


Figure 2. Block diagram of a simple stand-alone evolvable system.

3.3 Extreme Temperature Testbed

The purpose of this testbed is to achieve temperatures exceeding 350°C on the die of the FPTA-2 while staying below 280°C on the package. It is necessary to stay below 280°C on the package in order not to destroy the interconnects and package integrity. Die temperatures should stay below 400°C to make sure die attach epoxy does not soften and that the crystal structure of the aluminum core does not soften. To achieve these high temperatures the testbed includes an Air Torch system. The Air Torch is firing hot compressed air through a small hole of a high temperature resistance ceramic protecting the chip. To measure temperature Thermocouples were used.

Figure 3 shows the Air Torch apparatus electronically controlled by PID controller, which maintains a precision of ±10° C up to 1000° C. Figure 3 shows also the ceramic protecting the die connections and the package. The Temperature was measured above the die and under the die using thermocouples.

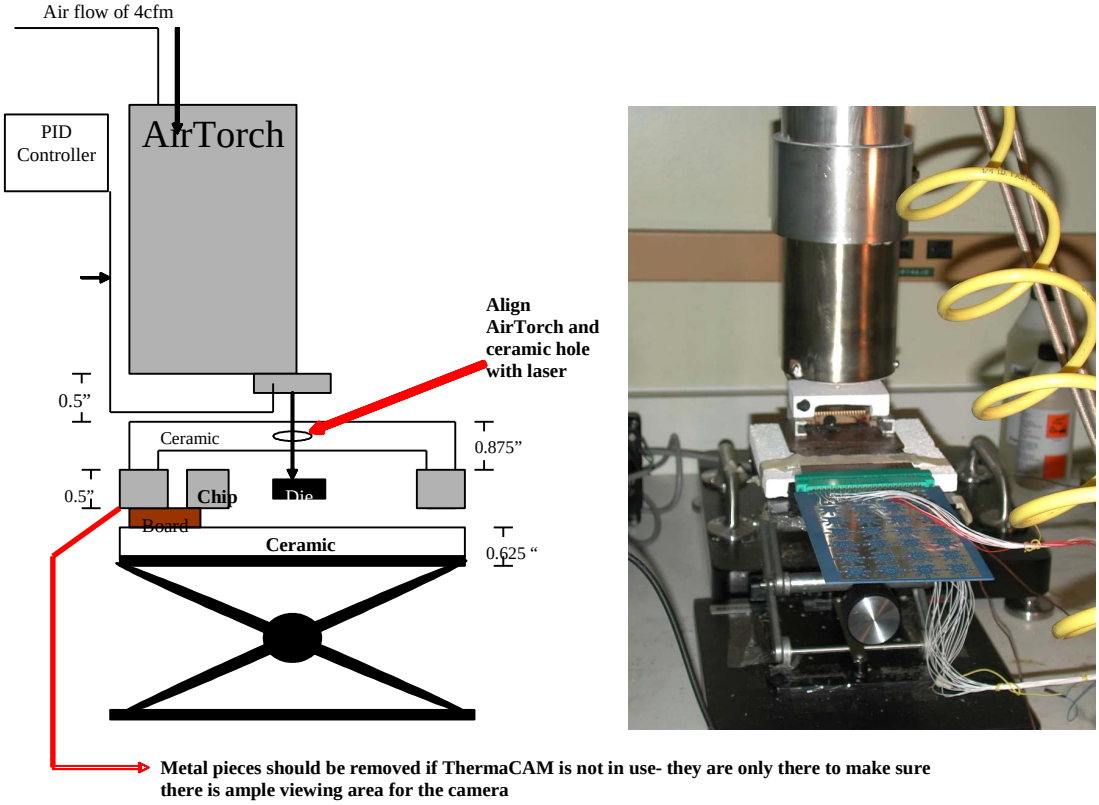


Figure 3. Experimental Setup for Extreme Temperature Experiments for the FPTA.

4. EXTREME TEMPERATURE EXPERIMENTS

We describe here experiments for evolutionary recovery of the functionality of the following circuits:

- Halfwave Rectifier at 280°C
- Closed Loop OpAmp at 245°C
- Low Pass Filters at 230°C
- High pass Filter at 230°C

The rationale of these experiments was of first evolving the proposed circuits at room temperature. After the functionality is achieved the temperature is increased using the apparatus shown in Figure 3, until the functionality is degraded. In order to recover the functionality, the evolutionary process is started again at high temperature. Therefore evolution can obtain a circuit that works at high temperature if the search process is carried on at the temperature in which the circuit is supposed to work.

4.1 Half wave rectifier on FPTA-2 at 280°C

The objective of this experiment is to recover functionality of a half wave rectifier for a 2kHz sine wave of amplitude 2V using only two cells of the FPTA-2 at 280°C. The fitness function given below does a simple sum of error between the target function and the output from the FPTA.

The input was a 2kHz excitation sine wave of 2V amplitude, while the target waveform was the rectified sine wave. The fitness function rewarded those individuals exhibiting behavior closer to target (by using a sum of differences between the response of a circuit and the target) and penalized those farther from it. The fitness function was:

$$F = \sum_{t_s=0}^{n-1} \begin{cases} R(t_s) - S(t_s) & \text{for } (t_s < n/2) \\ R(t_s) - V_{\max}/2 & \text{otherwise} \end{cases} \quad (1)$$

where $R(t_s)$ is the circuit output, $S(t_s)$ is the circuit stimulus, n is the number of sampled outputs, and V_{max} is 2V (the supply voltage). The output must follow the input during half-cycle, staying constant at a level of half way between the rails (1V) in the other half.

After the evaluation of 100 individuals, they were sorted according to fitness and a 9% (elite percentage) portion was set aside, while the remaining individuals underwent crossover (70% rate), either among themselves or with an individual from the elite, and then mutation (4% rate). The entire population was then reevaluated. Only two cells of the FPTA were allocated and used in this experiment.

Figure 4 depicts the response of the evolved circuit at room temperature and the degraded response at high temperature. Figure 5 shows the response of circuit obtained by running evolution at 280°C, where we can see that the functionality is recovered.

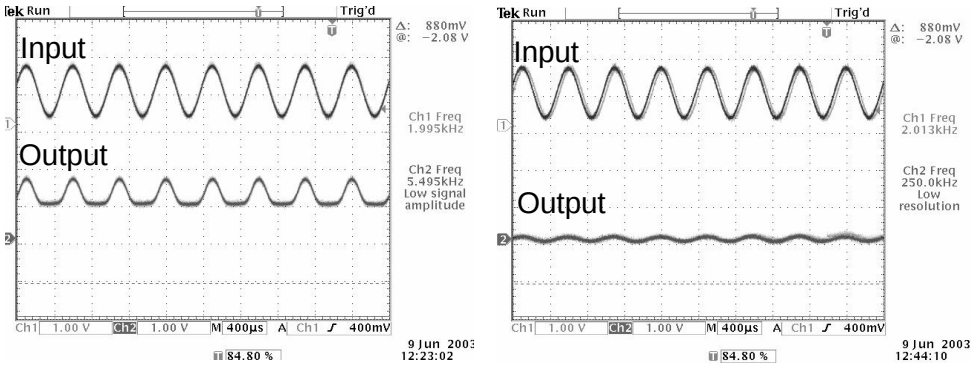


Figure 4: Input and output waves of the half-wave rectifier. At the left we show the response of the circuit evolved at 27°C. At the right we show the degraded response of the same circuit when the temperature is increased to 280°C.

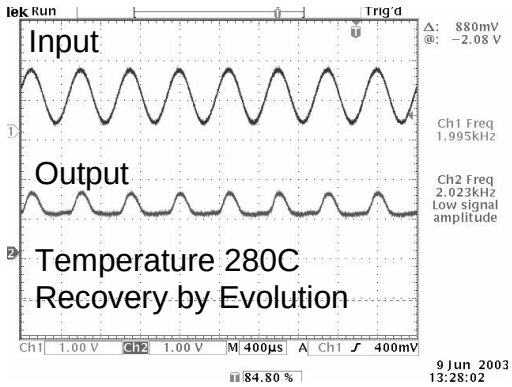


Figure 5 The solution for the Half wave rectifier at 280°C.

4.2 Amplifier circuit using closed loop OpAmp at 245°C

The objective of this experiment is to recover by evolution the functionality of a circuit that can provide a gain using compensation circuit introduced in the feedback loop of a conventional OpAmp implemented on the FPTA-2. Amplifiers are a very important building block in sensor circuits and it has been verified in this experiment that three FPTA cells can accomplish this task. One sine wave of 50mV amplitude and 1kHz frequency was applied as stimulus and the target output was a sine wave of twice the amplitude. The fitness encompassed the absolute sum of errors between the FPTA output, R(t), and the target, T(t) as shown below.

$$F = \sum_{t=0}^{n-1} \left| (R(t) - T(t)) \right| \qquad (2)$$

The other Evolutionary Algorithm parameters were similar to the ones described in the previous section.

Figure 6 illustrates the block diagram of the circuit in the FPTA-2 One cell of the chip implements a conventional OpAmp, while 3 re-configurable cells in a feedback loop have their configurations changed by evolution to achieve a compensating structure providing a voltage gain of 2.

Figure 7 shows the response of the circuit evolved at room temperature and the degraded functionality. Figure 8 depicts the recovered response of the circuit evolved at 245°C.

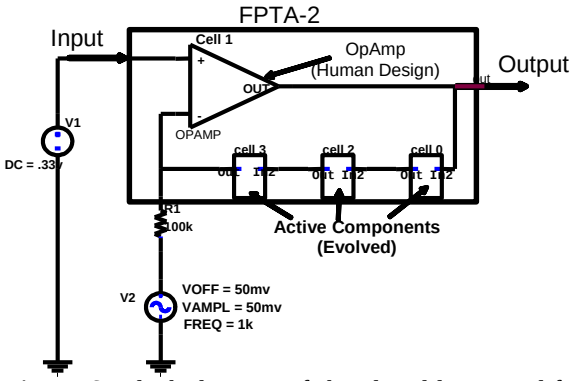
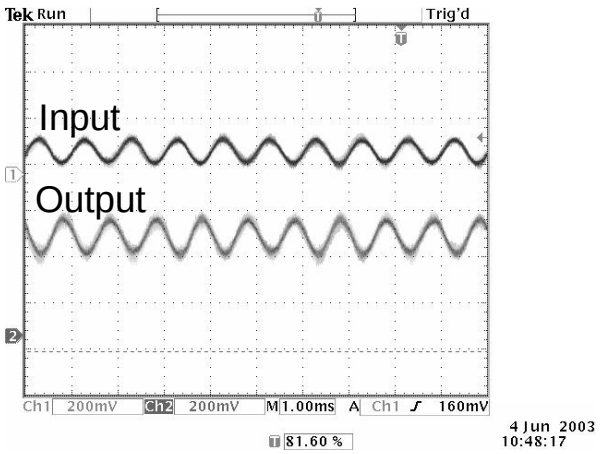


Figure 6: Block diagram of the closed-loop amplifier implemented in the FPTA-2. Cell 1 realizes a conventional OpAmp; cells 0, 2 and 3 are evolved to provide an amplification gain of 2.



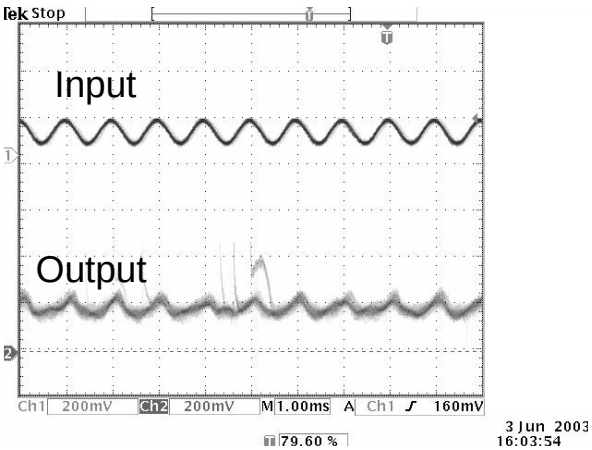


Figure 7 Degradation of the amplifier circuit. At the left response at room temperature, at the right response at 245°C.

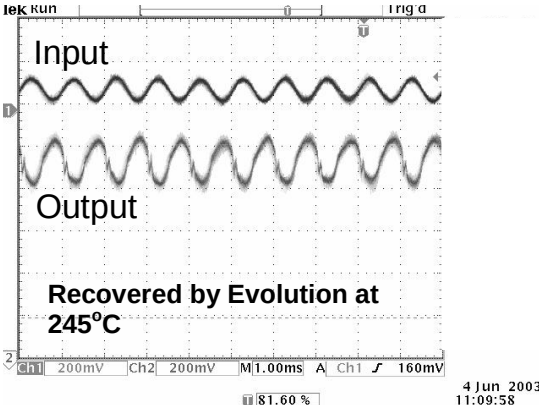


Figure 8: The solution for the recovered amplifier circuit

4.3 Low Pass filter at 230°C

The objective of this experiment is to recover the functionality of a low-pass filter given ten cells of the FPTA-2. The fitness function given below performs a sum of error between the target function and the output from the FPTA in the frequency domain.

$$F = \sum_{f_s=0}^{n-1} (R(f) - T(f)) \qquad (3)$$

Given two tones at 1kHz and 10kHz, the objective is to have at the output only the lowest frequency tone (1kHz). This hardware evolved circuit demonstrated that the FPTA-2 is able to recover active filters with some gain at 230°C. Figure 9 shows a view of the cell array in the FPTA-2 chip, with the 10 cells used in the experiment labeled from 0 to 9. The input is applied to several cells, while the output is taken from cell 9.

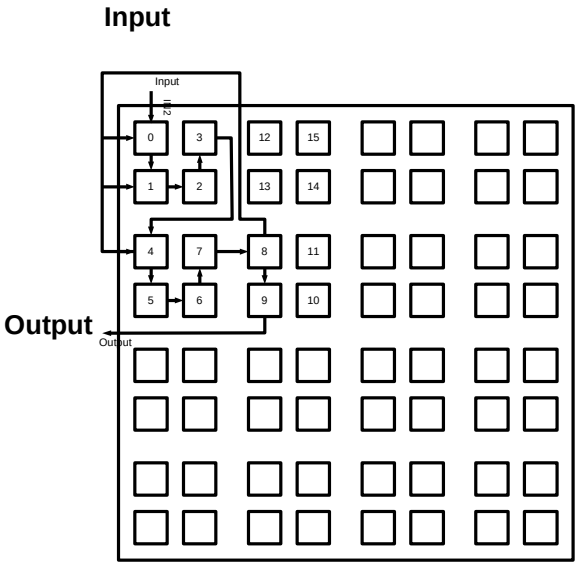


Figure 9: FPTA cells used in the low-pass filter experiment.

Figure 10 shows the response of the evolved filter at room temperature and degradation at 230°C. Figure 11 displays the same information in the frequency domain. Figure 12 shows the time and frequency response of the recovered circuit evolved at 230°C.

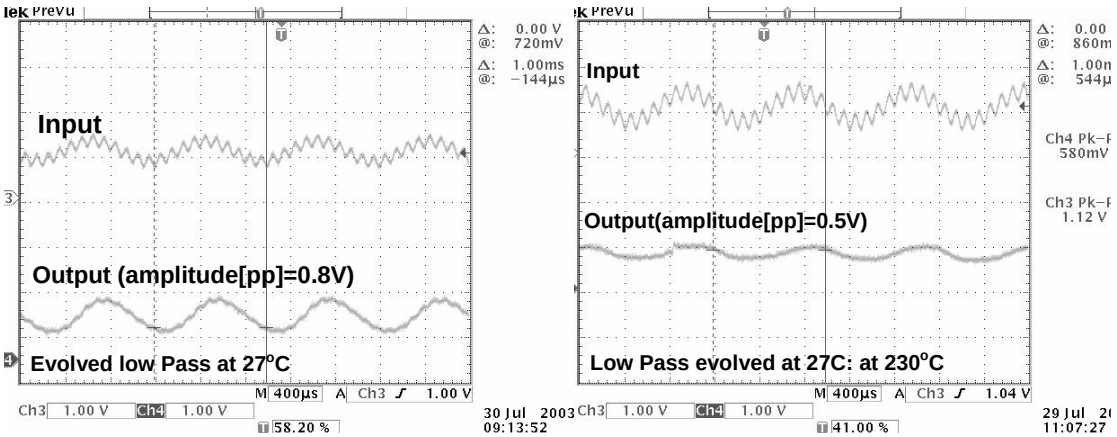


Figure 10: Low-Pass Filter. The graph in the left displays the input and output signals in the time domain. The graph in the right shows the input and output in the time domain when the FPTA-2 was submitted to temperature of 230°C (Circuit stimulated by two sine waves: 1kHz and 10kHz).

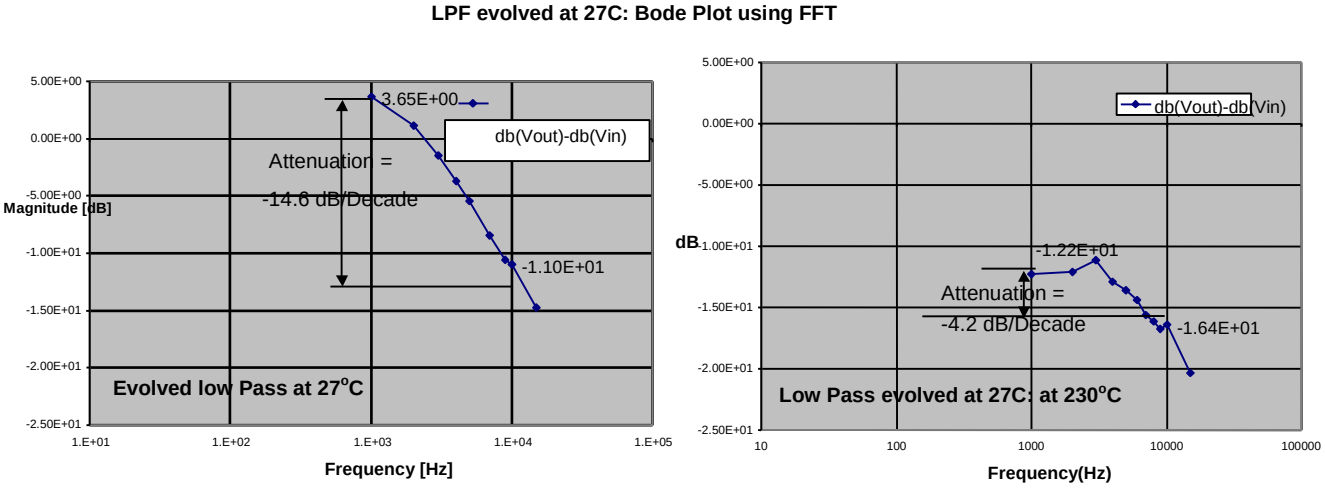


Figure 11: Low-Pass Filter. The graph in the left displays the frequency response of the output signal at room temperature. The graph in the right shows the frequency response of the output when the FPTA-2 was submitted to temperature of 230°C. (Circuit was stimulated by a sine wave with a frequency sweeping from 1kHz and 10kHz).

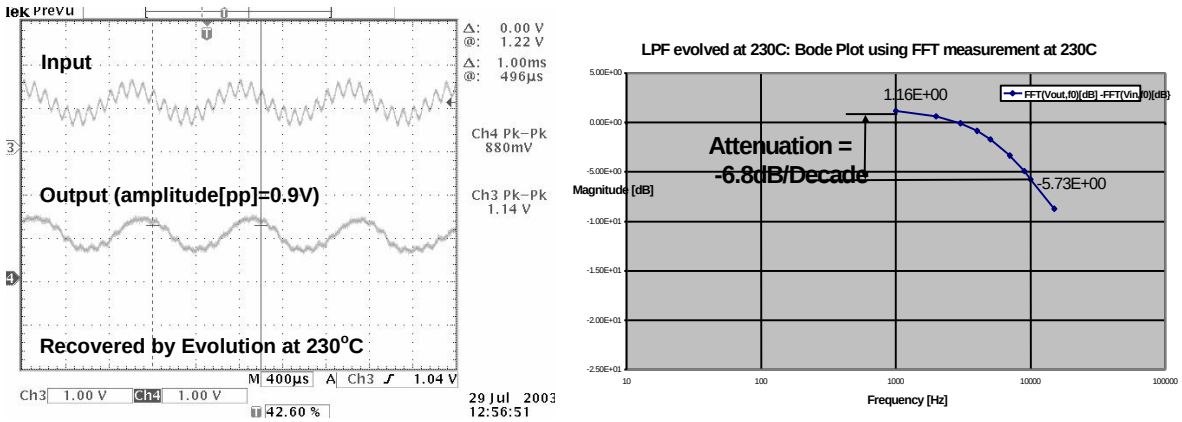


Figure12: Low-Pass Filter. The graph in the right displays the Bode diagram of the output signals. The graph in the left shows the circuit input stimulus and response in the time domain (Time response was obtained using a stimulation signal made of two sine waves: 1kHz and 10kHz – Frequency response was obtained by sweeping a frequency from 1kHz to 10kHz).

At room temperature, the originally evolved circuit presents a gain of 3dB at 1kHz and a roll-off of -14dB/dec. When the temperature is increased to 230°C, the roll-off goes to -4dB/dec and the gain at 1kHz falls to -12dB. In the recovered circuit at high temperature the gain at 1kHz is increased back to 1dB and the roll-off goes to -7dB/dec. Therefore the evolved solution at high temperature is able to restore the gain and to partially restore the roll-off.

4.4 High Pass filter at 230°C

The objective of this experiment is to recover the functionality of a high-pass filter using the same cells and configuration than for the low pass filter on the FPTA-2. Given two tones at 1kHz and 10kHz, the objective is to have at the output only the highest frequency tone (10kHz).

Figure 13 shows the response of the evolved filter at room temperature and degradation at 230°C. Figure 14 shows the response of the recovered circuit evolved at 230°C.

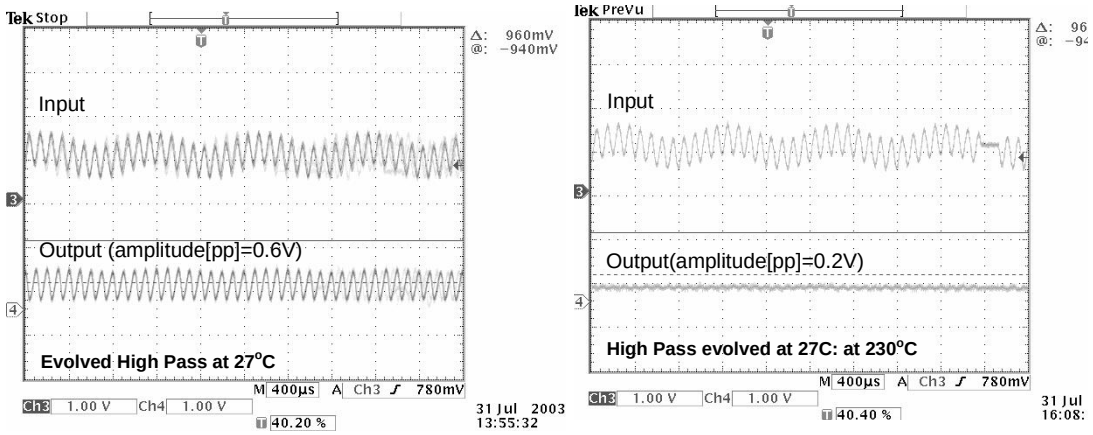


Figure 13: High-Pass Filter. The graph in the left displays the input and output signals in the time domain. The graph in the right shows the input and output signals when the FPTA-2 was submitted to temperature of 230°C (Circuit stimulated by the superposition of two sine waves: 1kHz and 10kHz).

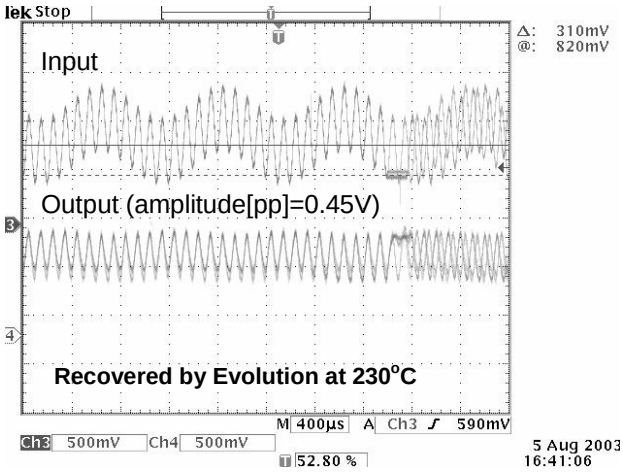


Figure 14: High-Pass Filter. The figure shows the circuit input stimulus and response in the time domain (Time response was obtained using a stimulation signal made of the superposition of two sine waves: 1kHz and 10kHz).

The originally evolved solution presented a roll-off of approximately 14dB/dec and a gain of -3dB at 10kHz. Both roll-off and gain were degraded when this solution was exposed to 230°C. The recovered solution at this temperature exhibited a roll-off of 7dB/dec and a -1dB gain at 10kHz.

5. DISCUSSION: TEMPERATURE LIMITATION OF THE SWITCH

We have performed a detailed analysis of the behavior of T-Gate switches of the FPTA-2 at high temperature. The switch is a key element for the evolutionary process since it modifies the topology of the circuit as a function of the signal applied to its gate and controlled by the chromosome. We have observed that the response of the device was independent of the chromosomes downloaded when the FPTA-2 was operated at 280°C or above.

Figure 15 illustrates the resistance of seven Tgates placed in series on the FPTA-2. At 125°C, the resistance of the Tgate in Off state is more than 1Gohm, while in On state it has a resistance of 31 kOhm. In comparison, when the FPTA-2 is warmed up to 280°C, the resistance of the Tgate is 60kOhm for On and Off State. The leakage currents between the nwell, pwell, Vdd and Ground makes the T-Gate switch behave at high temperature (over 250°C) as a low resistance independent of the signal applied to the T-Gate. These current leakages increase as the technology feature size decreases, being 0.18µ for FPTA-2 and 0.5µ for FPTA-0. As a consequence, we were able to recover functionality of circuit at higher temperature (320°C) using FPTA-0 [9].

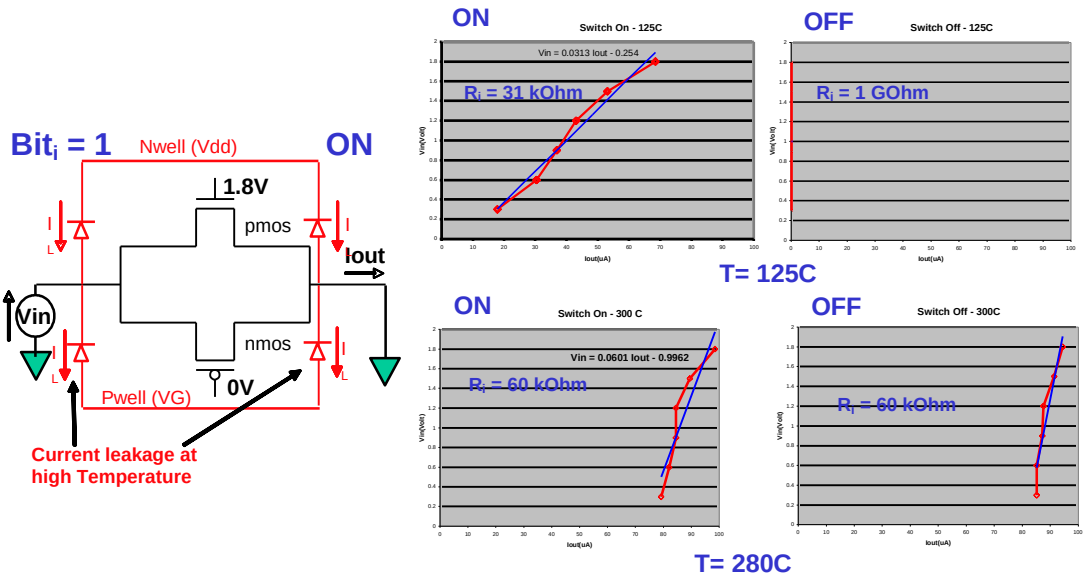


Figure 15 Current Leakage and behavior of Tgate at 125^{o}C and 250^{o}C in ON and OFF State

One way to partially overcome this problem is to increase the value of Vdd, which is also applied to the gate of the switch. For this particular technology the nominal Vdd value is 1.8V. By increasing the value of Vdd, the maximum temperature at which the T-gates can be controlled also increases (Figure 16). However this procedure also reduces the chip lifetime.

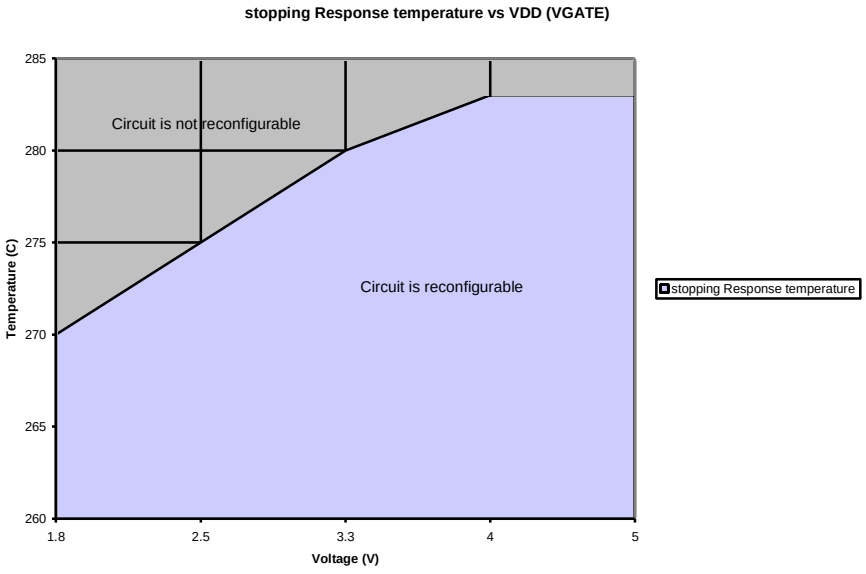


Figure 16: Maximum temperature that the FPTA can be reconfigured as Vdd is increased.

6. CONCLUSIONS

The experiments demonstrate the possibility of using evolutionary self-configuration to recover functionality lost at extreme temperatures. In addition, evolutionary design can be used to create designs targeted to the extreme temperatures. One should mention here that while a device may work at a certain temperature, the real limiting factors for applications will be failure rates and lifetimes. The experiments were performed on bulk CMOS because of the convenience and low cost of fabricating in this technology. For maximum performance, evolvable hardware should make use of an enhancing technique combined with materials/devices more appropriate for extreme temperatures, such as SiC, etc.

Acknowledgements

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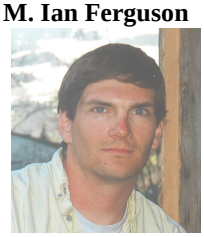

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